REMARKS

Claims 2-7, 9-13, and 19-21 are pending. Claims 2-7, 9-12, and 21 are rejected. Claims 13, 19, and 20 are allowed. Claims 2-4, 6, and 12-13 are amended. Claims 5 and 21 are canceled. Claims 22-23 are added. Reconsideration and allowance of Claims 2-4, 6-7, 9-13, 19-20, and 22-23 are respectfully requested.

Allowable Subject Matter

Claims 13, 19, and 20 are allowed. Applicant thanks the Examiner for the acknowledgement of allowable subject matter.

Objections to Claims

Claims 2, 3, 5, and 6 are objected to by the Examiner. Claim 5 has been canceled, and thus its objection is now moot. With respect to Claims 2, 3, and 6, Applicant has amended those claims in accordance with the Examiner's helpful comments, and requests that the objections to that Claims 2, 3, and 6 be withdrawn.

Rejection of Claims under 35 USC §112

Claims 2-7 and 21 are rejected under 35 USC §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the Applicant regards as the invention.

Claims 5 and 21 have been canceled, and thus their rejections are now moot.

With respect to Claim 4, the Examiner states that the limitation of "a plurality of first diode connected transistors connected in series" is confusing, and asks "are the transistors connected in series, or is more than one plurality implied, wherein those pluralities are connected in series?" Applicant disagrees.

The limitation in Claim 4 to which the Examiner refers recites, in whole, "a plurality of first diode connected transistors connected in series between the first input and a power supply voltage." As commonly used, the term "a plurality" means "a number more than one." Indeed, Applicant's specification states in paragraph [0031] that "FIG 5 has another aspect of the present invention showing the use of more than one series coupled diode-connected transistors on each of input of the comparator,

i.e., diode-connected transistors 322-1 to 322-N1 on node A and diode-connected transistors 324-1 to 324-M1 on node B, where N1 and M1 are positive numbers." Thus, the limitation "a plurality of first diode connected transistors connected in series between the first input and a power supply voltage" means that a number, greater than one, of diode connected transistors are connected in series between the first input and a power supply voltage, for example, as illustrated in Applicant's Fig. 5. Further, the term "at least one resistor divider," which is objected to by the Examiner, has been deleted from Claim 4. Accordingly, Applicant believes that Claim 4 is in compliance with 35 USC §112, second paragraph, and requests that the Examiner withdraw the present rejection of Claim 4.

Further, because Claims 2-3 depend from Claim 4, Applicant also requests that the Examiner withdraw the present rejection of Claims 2-3.

With respect to Claim 6, the Examiner states that it is not clear what is meant by "the hysteresis circuit configured to protect the power up reset circuit from glitches." In response thereto, Applicant has amended Claim 6 to recite that the hysteresis circuit is "configured to render the power up reset circuit less susceptible to noise in the power supply voltage or the ground potential." This limitation of Claim 6 is supported by language provided in paragraph [0036] of Applicant's specification[1]. Accordingly, Applicant believes that Claim 6 is now in compliance with 35 USC §112, second paragraph, and requests that the Examiner withdraw the present rejection of Claim 6.

Further, because Claim 7 depends from Claim 6, Applicant also requests that the Examiner withdraw the present rejection of Claim 7.

Rejection of Claims under 35 USC §102

Claims 2-4 are rejected under 35 USC §102(b) as being anticipated by U.S. Patent No. 4,309,627 to Tabata. Applicant respectively traverses these rejections.

Applicant's Claim 4, as amended, recites:

A power up reset circuit, comprising:

a comparator having first and second inputs and an output;

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1 The last sentence of paragraph [0036] states: "The hysteresis circuit makes the power up reset circuit far less susceptible to noise found on the supply or ground lines."

a plurality of first diode connected transistors connected in series between the first input and a power supply voltage;

a first resistor connected between the first input and ground potential;

a plurality of second diode connected transistors connected in series between the second input and ground potential; and

a reset signal generated at the output when the voltages at the first and second inputs are approximately the same.

Tabata's Fig. 6 shows two diode connected transistors (1-2) coupled between the power supply (Vdd) and the first comparator input (a), and a resistor divider circuit (8,9) coupled to the second comparator input (b). In contrast, Applicant's Claim 4 recites "a plurality of first diode connected transistors connected in series between the first input node and a power supply voltage," and "a plurality of second diode connected transistors connected in series between the second input and ground potential."

To anticipate a claim under 35 USC §102, each and every element of the claim must be disclosed in a single reference[2]. The exclusion of a claimed element, no matter how insubstantial or obvious, from a prior art reference is enough to negate anticipation under 35 USC §102.[3] Thus, because Tabata fails to disclose or suggest a power up reset circuit that includes "a plurality of first diode connected transistors connected in series between the first input node and a power supply voltage" and "a plurality of second diode connected transistors connected in series between the second input and ground potential," as recited in Applicant's Claim 4, Claim 4 is not anticipated by Tabata. Accordingly, Applicant respectfully requests the Examiner to withdraw the rejection of Claim 4.

Applicant notes that because the recitation of "a plurality of second diode connected transistors connected in series between the second input and ground potential" in Claim 4 appears in original Claim 5, the amendment of Claim 4 does not introduce new matter, and does not necessitate a new search by the Examiner.

Claims 2-3 depend from Claim 4 and therefore distinguish over the cited

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2 Corning Glass Works v. Sumitomo Electric, 9 USPQ2d 1962, 1965 (Fed. Cir. 1989).
3 Connell v. Sears, Roebuck & Co., 220 USPQ 193, 198 (Fed. Cir. 1983).

references for at least the same reasons as Claim 4.

Rejection of Claims under 35 USC §103 (Frisch)

Claims 2-5 are rejected under 35 USC §103(a) as being unpatentable over U.S. Patent No. 5,144,159 to Frisch. Claim 5 is canceled, and thus its rejection is now moot. Applicant respectively traverses the rejections of Claims 2-4.

Applicant's Claim 4, as amended, recites:

A power up reset circuit, comprising:

a comparator having first and second inputs and an output;

a plurality of first diode connected transistors connected in series between the first input and a power supply voltage;

a first resistor connected between the first input and ground potential;

a plurality of second diode connected transistors connected in series between the second input and ground potential; and

a reset signal generated at the output when the voltages at the first and second inputs are approximately the same.

The Examiner notes that Frisch fails to "show a plurality of first diode connected transistors 24," and then states that "it would have been obvious to one of ordinary skill in the art to replace single transistor 24 with a plurality of series connected transistors that are each diode connected, thus rendering claim 4 obvious." Applicant disagrees.

The PTO has the burden of establishing a prima facie case of obviousness under 35 USC §103. It must show that some objective teaching in the prior art generally held by one of ordinary skill in the art would lead an individual to combine the relevant teachings of the references[4]. It is well settled that there must be some reason or motivation in the art to combine or modify references when making a prima facie case of obviousness under 35 USC 103. Thus, absent some teaching in the art to modify a reference, the Examiner has failed to establish a prima facie case for obviousness. Accordingly, since the Examiner has failed to point to any language in Frisch that teaches or suggests "a plurality of first diode connected transistors connected in series between the first input node and a power supply voltage," as

4 In re Fine, 837 F.2d 1071, 1074 (Fed. Cir. 1988).

recited in Applicant's Claim 4, Claim 4 is patentable over the cited references. Further, Frisch also fails to disclose or suggest "a plurality of second diode connected transistors connected in series between the second input and ground potential," as recited in Applicant's Claim 4, and therefore Claim 4 is not obvious over Frisch.

The Examiner states that "it appears that the applicant does not believe one of ordinary skill in the art would know that the number of series coupled diode connected transistors can be changed to change the overall threshold (or voltage) drop across the transistors," and cites several references (i.e., Woods, Payne, and Kitade) showing that multiple diode-connected transistors may be connected in series to achieve a desired voltage drop. However, there is no language in Frisch that suggests or teaches a plurality of diode-connected transistors connected in series between the first input node and a power supply voltage" and "a plurality of second diode connected transistors connected in series between the second input and ground potential," as recited in Applicant's Claim 4. Thus, absent some teaching in Frisch to modify the circuit of Frisch as proposed by the Examiner, the Examiner has not made a prima facie case of obviousness, and therefore Claim 4 is not obvious over Frisch.

In addition Frisch teaches away from a plurality of diode-connected transistors connected in series. Looking at Figure 5 of Frisch, FET 51 is the single diode connected transistor. As Vdd increases in voltage such that it is above the threshold voltage of FET 51, FET 51 is enabled and conduction from Vdd through FETs 51 and 52 begins. This causes the voltage of terminal 56 to track exactly one threshold voltage below the instantaneous value of Vdd as Vdd rises, until Vdd reaches the exemplary +5 volts (col. 6, lines 20-26). Figure 5 is the preferred embodiment and circuit A2 corresponds to circuit A1 in Figure 4 (col. 4, lines 43-55). Thus Frisch teaches the use of only one diode connected transistor.

Claims 2-3 depend from Claim 4 and therefore distinguish over the cited references for at least the same reasons as Claim 4.

Rejection of Claims under 35 USC §103 (Degoirat)

Claims 6-7 are rejected under 35 USC §103(a) as being unpatentable over Tabata in view of U.S. Patent No. 6,147,521 to Degoirat et al. Applicant respectively

traverses these rejections.

Claims 6-7 depend from Claim 4 and therefore distinguish over the cited references for at least the same reasons as Claim 4.

Rejection of Claims under 35 USC §103 (Guritz)

Claims 2-5 are rejected under 35 USC §103(a) as being unpatentable over U.S. Patent No. 4,142,118 Guritz. Claim 5 is canceled, and thus its rejection is now moot. Applicant respectively traverses the rejections of Claims 2-4.

The Examiner notes that Guritz fails to disclose "a plurality of diode connected transistors connected in series between an input and either a power supply voltage or ground potential," and then states that "one of ordinary skill in the art would realize that Fig. 4a could comprise a plurality of series coupled diode connected transistors T1 coupled between VDD and VR, with VR connected to the first input." Applicant disagrees.

Although it is possible to replace the single diode connected transistor T1 of Guritz with a plurality of diode connected transistors, there must be some motivation in the art to do so. Indeed, as noted above, The PTO has the burden of establishing a prima facie case of obviousness under 35 USC §103, and absent some teaching in the art to modify a reference, the Examiner has failed to establish a prima facie case for obviousness. Accordingly, since the Examiner has failed to point to any language in Guritz that teaches or suggests "a plurality of first diode connected transistors connected in series between the first input node and a power supply voltage" and "a plurality of second diode connected transistors connected in series between the second input and ground potential," as recited in Applicant's Claim 4, Claim 4 is patentable over the cited references.

Claims 2-3 depend from Claim 4 and therefore distinguish over the cited references for at least the same reasons as Claim 4.

Rejection of Claims under 35 USC §103 (Furuchi)

Claims 9-12 are rejected under 35 USC §103(a) as being unpatentable over Guritz or Frisch in view of U.S. Patent No. 6,121,813 to Furuchi. Applicant respectively

traverses these rejections.

Applicant's Claim 12 recites:

An integrated circuit having a power up reset circuit, comprising:

a power supply directly connected to a first resistor, the first resistor in series with a first input node and a first diode connected transistor, the first diode connected transistor coupled to ground;

a second diode connected transistor directly connected to the power supply and connected in series with a second input node and a second resistor, wherein the second resistor is directly connected to ground; and

a comparator connected to the first input node and second input node and producing a reset signal when the voltages at the first and second input nodes are about equal, wherein the reset signal is at an output node between a first capacitor connected to the power supply and a second capacitor connected to ground.

First, Furuchi discloses a delay circuit, NOT a power up reset circuit.

The delay circuit of Furuchi includes an integrating circuit 104 having a resistor 7 coupled to a delay line, a first capacitor C1 coupled between the delay line and VDD, and a second capacitor C2 coupled between the delay line and ground potential (see col. 5, lines 52-58). In operation, the integrating circuit 104 integrates an input signal to smooth its waveform (see col. 5, lines 61-65).

The Examiner states that "it would have been obvious to one of ordinary skill in the art to apply the teaching of Furuchi to the circuit of Guritz. In this case, it would have been obvious to couple first capacitor C1 between output node 16 (of Guritz) and power supply VDD, and couple second capacitor C2 between output node 16 and ground, thus rendering claims 11 and 12 obvious." The Examiner also states that it would have been obvious to one of ordinary skill in the art to apply the teaching of Furuchi to the circuit of Frisch. Applicant disagrees.

It appears that the Examiner is improperly using hindsight of Applicant's invention to modify the circuits of Guritz or Frisch to include the teachings of Furuchi. However, there is no language in Guritz or Frisch that suggests or teaches including "a first capacitor connected to the power supply and a second capacitor connected to ground," as recited in Applicant's Claim 12, nor has the Examiner pointed to any such

language in Guritz or Frisch. Thus, absent some teaching in the art to combine references (as proposed by the Examiner) to arrive at the invention recited in Applicant's Claim 12, the Examiner has not made a prima facie case of obviousness under 35 USC §103, and therefore Applicant respectfully requests the Examiner to withdraw the rejection of Claim 12.

Claims 9-11 and 23 depend from Claim 12 and therefore distinguish over the cited references for at least the same reasons as Claim 12.

New Claims

New Claim 22 depends from Claim 4, and therefore distinguishes over the cited references for at least the same reasons as Claim 4. New Claim 23 depends from Claim 12, and therefore distinguishes over the cited references for at least the same reasons as Claim 4. Further, Claims 22 and 23 each recite subject matter similar to that recited in allowed Claim 13, and thus are also allowable over the cited references for the same reasons as Claim 13.

CONCLUSION

In light of the above remarks, it is believed that Claims 2-4, 6-7, 9-13, 19-20, and 22-23 are in condition for allowance and, therefore, a Notice of Allowance of Claims 2-4, 6-7, 9-13, 19-20, and 22-23 is respectfully requested. If the Examiner's next action is other than allowance as requested, the Examiner is requested to call the undersigned at (408) 879-6149.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to: Commissioner for Patents, P.O. BOX 1450, Alexandria, VA 22313-1450, on May 6, 2005.

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Name

Signature